IN THE CLAIMS:

Please amend claims 38 and 44-49 as indicated in the following.

Claims Listing:

1. – 37. (Canceled)

38. (Currently Amended) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

receiving said instruction;

decoding said instruction;

providing to said coprocessor, at least partially coincident with said decoding:

at least a predetermined portion of said instruction[[,]] via a first portion of said coprocessor bus[[,]]; and

a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus; and

receiving from said coprocessor, a second control signal indicating said predetermined portion of said instruction caused an exception within said coprocessor.

39. (Previously Presented) The method of claim 38, wherein the second control signal is received prior to said processor completing said instruction.

40. (Previously Presented) The method of claim 38, further comprising discarding said instruction.

41. (Previously Presented) The method of claim 40, further comprising negating the first control signal.

42. (Previously Presented) The method of claim 40, further comprising providing a third control signal to said coprocessor bus to indicate when execution of said instruction is proceeding, wherein if the first control signal is negated, the third control signal is not asserted.

43. (Previously Presented) The method of claim 38, further comprising providing a third control signal to said coprocessor bus to indicate when execution of said instruction is proceeding, wherein if the first control signal is asserted, the third control signal is asserted.

44. (Currently Amended) A method for a coprocessor to perform an operation in response to an instruction received by a processor coupled to said coprocessor via a coprocessor bus, the method comprising:

receiving from said processor[[,]]:

at least a predetermined portion of said instruction via a first portion of said coprocessor bus; and

a first control signal indicating that said instruction is being decoded by said processor[[,]] via a second portion of said coprocessor bus;

initiating execution of said instruction; and

providing to said processor a second control signal indicating said instruction caused an exception.

45. (Currently Amended) The method of claim 44, wherein said second control signal is provided to said processor prior to said instruction completing in said processor.

46. (Currently Amended) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

in said processor:

receiving said instruction;

decoding said instruction; and

providing to said coprocessor, at least partially coincident with said decoding[[,]]:

at least a predetermined portion of said instruction, via a first portion of said coprocessor bus[[,]]; and

a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus;

in said coprocessor:

receiving from said processor[[,]]:

the predetermined portion of said instruction[[,]] via the first portion of said coprocessor bus[[,]]; and

the first control signal[[,]]; and

providing to said processor a second control signal indicating said instruction caused an exception[[,]] via a third portion of said coprocessor bus.

47. (Currently Amended) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

receiving said instruction;

decoding said instruction;

providing to said coprocessor, at least partially coincident with said decoding:

at least a predetermined portion of said instruction, via a first portion of said coprocessor bus[[,]]; and

a first control signal indicating that said instruction is being decoded by saidprocessor via a second portion of said coprocessor bus; and

receiving from said coprocessor, a second control signal indicating whether said predetermined portion of said instruction caused an exception within said coprocessor.

48. (Currently Amended) A method for a coprocessor to perform an operation in response to an instruction received by a processor coupled to said coprocessor via a coprocessor bus, the method comprising:

receiving from said processor[[,]]:

at least a predetermined portion of said instruction via a first portion of said coprocessor bus; and

a first control signal indicating that said instruction is being decoded by said processor[[,]] via a second portion of said coprocessor bus;

initiating execution of said instruction; and

providing to said processor a control signal indicating whether said instruction caused an exception.

49. (Currently Amended) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

in said processor:

receiving said instruction;

decoding said instruction; and

providing to said coprocessor, at least partially coincident with said decoding[[,]]

at least a predetermined portion of said instruction[[,]] via a first portion of said coprocessor bus[[,]]; and

a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus;

in said coprocessor:

receiving from said processor[[,]]:

the predetermined portion of said instruction[[,]] via the first portion of said coprocessor bus[[,]]; and

the first control signal[[,]]; and

providing to said processor a second control signal indicating whether said instruction caused an exception[[,]] via a third portion of said coprocessor bus.